John T. Anderson

Engineering Note

Date: June 21,2001
Rev Date: June 21,2001

Project: New MCM (MCM II)
Doc. No: a1010621

Subject: Details of interface between existing AFE Revision 1C board and new MCM device

Introduction

This document describes the detailed implementation of the new MCM pinout and the methods by which this new MCM will connect to the AFE board. It is predicated on the architecture proposed by M. Johnson, B. Hoeneisen & P. Rubinov in which a new 64-channel discriminator chip is connected to two commercial FADC chips and a small FPGA. The FADC/FPGA is assumed to replace all SVX and VSVX functionality, plus the FPGA is also to replace the LVDS_MUX functionality of the AFE board.

This document concludes that the AFE board will be ***radically*** modified. My engineering opinion is that the amount of rework required to make the new MCM shoehorn into the AFE is large and risky. At minimum, the following will occur:

- The Virtual SVX (VSVX) CPLD will be removed or reduced to a simple interconnect with no logic within it. All VSVX functionality will be subsumed into the FPGAs of the new MCM.
- All FIFO components associated with the AFE implementation of the VSVX are removed for power savings, in case the new MCM dissipates more heat than the old one.
- All VSVX_MUX CPLD components on the AFE are removed for power savings, by the same reasoning.
- All LVDS_MUX CPLD components on the AFE are retained but the programming is completely redesigned such that the LVDS_MUX is merely a connection device and/or control register will all LVDS multiplexing of discriminator data subsumed into the FPGAs of the new MCM.
- All 10ELT20 differential PECL clock drivers for the SVX chips in the old MCMs will be removed. The input pin will be physically shorted to the positive output pin and terminations repositioned such that the SVX clock will be presented no longer as a differential PECL signal but a single-ended TTL signal.
- The CLOCKGEN CPLD of the AFE will be completely redesigned so that all SIFT clock signals are removed and replaced by a distribution of 53 MHz, 61MHz and 7.6 MHz clocks for the new MCMs. The 7.6 MHz clock will be provided as a pulse-width-modulated (PWM) clock such that the 'high' time indicates the acquisition time for the new discriminator and the 'low' time indicates the reset interval.

Power Considerations

Even at this early stage of design, a great deal of rework is being considered for the AFE boards, including a large number of added wires. The reliability of an AFE board with that much rework is questionable. A new AFE board design is probably necessary unless the new MCM design is reworked to use +5V instead of +3.3V. A more difficult problem is the total power distribution of the system. At present the AFE board is supplied +5V, +3.3V, +5.5V, +12V and –12V. The production implementation utilizes approximately 80% of the maximum bulk power supply limit for both +5V and +3.3V, and about 70% of the maximum bulk power supply limit for the +5.5V. The new MCM will require +2.5V and +3.3V power. AFE power distribution creates +5V and +3.5V at limited current from the +5.5V supply, with digital, high-current supplies coming from the +5V. The bulk +3.3V supply is not routed to the area of the board where the MCMs reside. At maximum, only 350 mA of total +5.5V power per MCM is available.

Although linear regulators are available in the correct pinout to create +2.5V and +3.3V from the +5.5V supply, no such drop-in replacement is available from the +5V. I consider it highly unlikely that the entire MCM can be run on 250 mA of +3.3V and 100mA of +2.5V power.

Functional Details of Interfaces to new MCM

1. The 64 charge inputs of the old MCM are used as the 64 charge inputs of the new MCM. Note that the table below correlates which pin of the MCM is which SVX channel to facilitate matching the functionality of the new MCM to the old MCM to greatest possible degree.
2. The present power distribution to the MCM provides two +5V MOSFET switch inputs, two fixed output linear regulators with a outputs of 5V/3.5V respectively, both limited to 150mA and one resistor-set linear regulator with a maximum output of 5.2V/150mA. It is assumed here that the adjustable linear is re-set to provide 2.5V and the other two are ***removed and replaced*** by new parts of the same pinout to generate two 3.3V, 150mA supplies. Of course, *the maximum power output of the regulators sums to more than the bulk power supply for the system can provide.* As earlier stated, the best one can hope for is a total of 325 – 350 mA from the +5.5V power, meaning that the +2.5V has to run at less than 150 mA, more like 50mA.
3. The threshold/VREF DACs of the current AFE can be re-used to some degree to provide a better VCAL function for internal test modes of the new MCM.
4. Download of the FPGA program upon power up is performed using the parallel mode, where the micro reads data from a new configuration EPROM and writes it through the LVDS_MUX CPLD to the new FPGA. *This implies yet another modification to the AFE – a daughter board connected to J5 where the configuration EPROM would reside, plus code changes to the 1553 PLD to allow the micro to read the EPROM.*
5. The PWM clock required by the new discriminator is created by the CLOCKGEN. Other SIFT clock lines are used to distribute the 53 MHz and 61 MHz clocks needed by the FPGA.

MCM Pinout Table

The following table goes through all 228 pins of the MCM and details what each does now, and what it will do in the new MCM.

MCM Pin(s)	Function in old MCM	Notes on AFE implementation	Proposed usage in New MCM
1	Charge input, Flex Cable channel #14; SVX Channel #88	AC coupled to board input thru 100pF	Same as in old MCM
2	Charge input, Flex Cable channel #13; SVX Channel #91	AC coupled to board input thru 100pF	Same as in old MCM
3	Charge input, Flex Cable channel #11; SVX Channel #92	AC coupled to board input thru 100pF	Same as in old MCM
4	Charge input, Flex Cable channel #12; SVX Channel #94	AC coupled to board input thru 100pF	Same as in old MCM
6	Charge input, Flex Cable channel #16; SVX Channel #97	AC coupled to board input thru 100pF	Same as in old MCM
7	Charge input, Flex Cable channel #15; SVX Channel #98	AC coupled to board input thru 100pF	Same as in old MCM
8	Charge input, Flex Cable channel #23; SVX Channel #99	AC coupled to board input thru 100pF	Same as in old MCM
9	Charge input, Flex Cable channel #27;	AC coupled to board input thru 100pF	Same as in old MCM

	SVX Channel #102		
10	Charge input, Flex Cable channel #28; SVX Channel #103	AC coupled to board input thru 100pF	Same as in old MCM
11	Charge input, Flex Cable channel #25; SVX Channel #104	AC coupled to board input thru 100pF	Same as in old MCM
13	Charge input, Flex Cable channel #33; SVX Channel #107	AC coupled to board input thru 100pF	Same as in old MCM
14	Charge input, Flex Cable channel #37; SVX Channel #108	AC coupled to board input thru 100pF	Same as in old MCM
15	Charge input, Flex Cable channel #32; SVX Channel #109	AC coupled to board input thru 100pF	Same as in old MCM
16	Charge input, Flex Cable channel #36; SVX Channel #110	AC coupled to board input thru 100pF	Same as in old MCM
17	Charge input, Flex Cable channel #44; SVX Channel #111	AC coupled to board input thru 100pF	Same as in old MCM
18	Charge input, Flex Cable channel #41; SVX Channel #112	AC coupled to board input thru 100pF	Same as in old MCM
20	Charge input, Flex Cable channel #42; SVX Channel #117	AC coupled to board input thru 100pF	Same as in old MCM
21	Charge input, Flex Cable channel #46; SVX Channel #118	AC coupled to board input thru 100pF	Same as in old MCM
22	Unused MCM Input Pin (live SIFT input, tied to an SVX channel, unused)	Tied to AGND plane thru 100pF	No Connection
23	Unused MCM Input Pin (live SIFT input, tied to an SVX channel, unused)	Tied to AGND plane thru 100pF	No Connection
24	Unused MCM Input Pin (live SIFT input, tied to an SVX channel, unused)	Tied to AGND plane thru 100pF	No Connection
25	Unused MCM Input Pin (live SIFT input, tied to an SVX channel, unused)	Tied to AGND plane thru 100pF	No Connection
171	Unused MCM Input Pin (live SIFT input, tied to an SVX	Tied to AGND plane thru 100pF	No Connection

	channel, unused)		
172	Unused MCM Input Pin (live SIFT input, tied to an SVX channel, unused)	Tied to AGND plane thru 100pF	No Connection
173	Unused MCM Input Pin (live SIFT input, tied to an SVX channel, unused)	Tied to AGND plane thru 100pF	No Connection
174	Unused MCM Input Pin (live SIFT input, tied to an SVX channel, unused)	Tied to AGND plane thru 100pF	No Connection
175	Charge input, Flex Cable channel #53; SVX Channel #10	AC coupled to board input thru 100pF	Same as in old MCM
176	Charge input, Flex Cable channel #51; SVX Channel #11	AC coupled to board input thru 100pF	Same as in old MCM
178	Charge input, Flex Cable channel #56; SVX Channel #12	AC coupled to board input thru 100pF	Same as in old MCM
179	Charge input, Flex Cable channel #64; SVX Channel #13	AC coupled to board input thru 100pF	Same as in old MCM
180	Charge input, Flex Cable channel #61; SVX Channel #16	AC coupled to board input thru 100pF	Same as in old MCM
181	Charge input, Flex Cable channel #67; SVX Channel #17	AC coupled to board input thru 100pF	Same as in old MCM
182	Charge input, Flex Cable channel #68; SVX Channel #20	AC coupled to board input thru 100pF	Same as in old MCM
183	Charge input, Flex Cable channel #65; SVX Channel #21	AC coupled to board input thru 100pF	Same as in old MCM
185	Charge input, Flex Cable channel #73; SVX Channel #22	AC coupled to board input thru 100pF	Same as in old MCM
186	Charge input, Flex Cable channel #77; SVX Channel #23	AC coupled to board input thru 100pF	Same as in old MCM
187	Charge input, Flex Cable channel #72; SVX Channel #26	AC coupled to board input thru 100pF	Same as in old MCM
188	Charge input, Flex Cable channel #78; SVX Channel #27	AC coupled to board input thru 100pF	Same as in old MCM
189	Charge input, Flex	AC coupled to board input thru	Same as in old MCM

	Cable channel #75; SVX Channel #28	100pF	
190	Charge input, Flex Cable channel #81; SVX Channel #29	AC coupled to board input thru 100pF	Same as in old MCM
192	Charge input, Flex Cable channel #87; SVX Channel #32	AC coupled to board input thru 100pF	Same as in old MCM
193	Charge input, Flex Cable channel #82; SVX Channel #36	AC coupled to board input thru 100pF	Same as in old MCM
194	Charge input, Flex Cable channel #85; SVX Channel #37	AC coupled to board input thru 100pF	Same as in old MCM
195	Charge input, Flex Cable channel #86; SVX Channel #38	AC coupled to board input thru 100pF	Same as in old MCM
196	Charge input, Flex Cable channel #88; SVX Channel #41	AC coupled to board input thru 100pF	Same as in old MCM
197	Charge input, Flex Cable channel #83; SVX Channel #42	AC coupled to board input thru 100pF	Same as in old MCM
199	Charge input, Flex Cable channel #84; SVX Channel #43	AC coupled to board input thru 100pF	Same as in old MCM
200	Charge input, Flex Cable channel #76; SVX Channel #46	AC coupled to board input thru 100pF	Same as in old MCM
201	Charge input, Flex Cable channel #71; SVX Channel #47	AC coupled to board input thru 100pF	Same as in old MCM
202	Charge input, Flex Cable channel #74; SVX Channel #48	AC coupled to board input thru 100pF	Same as in old MCM
203	Charge input, Flex Cable channel #66; SVX Channel #49	AC coupled to board input thru 100pF	Same as in old MCM
204	Charge input, Flex Cable channel #62; SVX Channel #52	AC coupled to board input thru 100pF	Same as in old MCM
206	Charge input, Flex Cable channel #63; SVX Channel #53	AC coupled to board input thru 100pF	Same as in old MCM
207	Charge input, Flex Cable channel #55; SVX Channel #56	AC coupled to board input thru 100pF	Same as in old MCM
208	Charge input, Flex Cable channel #58; SVX Channel #57	AC coupled to board input thru 100pF	Same as in old MCM

209	Charge input, Flex Cable channel #52; SVX Channel #58	AC coupled to board input thru 100pF	Same as in old MCM
210	Charge input, Flex Cable channel #57; SVX Channel #59	AC coupled to board input thru 100pF	Same as in old MCM
211	Charge input, Flex Cable channel #54; SVX Channel #62	AC coupled to board input thru 100pF	Same as in old MCM
213	Charge input, Flex Cable channel #45; SVX Channel #66	AC coupled to board input thru 100pF	Same as in old MCM
214	Charge input, Flex Cable channel #48; SVX Channel #67	AC coupled to board input thru 100pF	Same as in old MCM
215	Charge input, Flex Cable channel #47; SVX Channel #68	AC coupled to board input thru 100pF	Same as in old MCM
216	Charge input, Flex Cable channel #43; SVX Channel #71	AC coupled to board input thru 100pF	Same as in old MCM
217	Charge input, Flex Cable channel #35; SVX Channel #72	AC coupled to board input thru 100pF	Same as in old MCM
218	Charge input, Flex Cable channel #38; SVX Channel #73	AC coupled to board input thru 100pF	Same as in old MCM
220	Charge input, Flex Cable channel #31; SVX Channel #74	AC coupled to board input thru 100pF	Same as in old MCM
221	Charge input, Flex Cable channel #34; SVX Channel #77	AC coupled to board input thru 100pF	Same as in old MCM
222	Charge input, Flex Cable channel #26; SVX Channel #78	AC coupled to board input thru 100pF	Same as in old MCM
223	Charge input, Flex Cable channel #22; SVX Channel #81	AC coupled to board input thru 100pF	Same as in old MCM
224	Charge input, Flex Cable channel #21; SVX Channel #82	AC coupled to board input thru 100pF	Same as in old MCM
225	Charge input, Flex Cable channel #24; SVX Channel #83	AC coupled to board input thru 100pF	Same as in old MCM
227	Charge input, Flex Cable channel #18; SVX Channel #84	AC coupled to board input thru 100pF	Same as in old MCM
228	Charge input, Flex	AC coupled to board input thru	Same as in old MCM

	Cable channel #17; SVX Channel #87	100pF	
67,68,128,129	VDD_A power input	Fixed linear regulator, nominal +5V, 150 mA maximum current.	Suggest replacing current TK11350 regulator with TK11333 component; provides +3.3V power for FPGA.
78,79,111,112	VDD_D power input	Unregulated +5V digital supply, limited to 1A	No connection
89	AVDD power input	Resistor-adjustable linear regulator, nominal +5.2V, 150 mA maximum current.	Change AFE resistor values to yield +2.5V, for use as VDD for new discriminator chip
87	AVDD2 power input	Fixed linear regulator, nominal +3.5V, 150 mA maximum current.	Suggest replacing current TK11235 regulator with TK11333 component; provides +3.3V power for FADCs.
107	DVDD power input	Unregulated +5V digital supply, limited to 200mA	No connection
27,46,65,77,80, 110,113,119, 131,150,169	Digital Ground	All pins tied directly to DGND return plane	Same as in old MCM
5,12,19,26,66, 76,85,120,127, 130,170,177, 184,191,198, 205,212,219, 226	Analog Ground	All pins tied directly to AGND return plane	Same as in old MCM
86,88	SVX AGND	Tied via 0 ohm resistors to AGND return plane and/or DGND return plane; nominally, both resistors installed	Use as desired for “clean” AGND connection for discriminator chip; remove 0 ohm resistor to DGND plane, replace 0 ohm resistor to AGND plane with SMT inductor.
106	SVX DGND	Tied via 0 ohm resistors to AGND return plane and/or DGND return plane; nominally, both resistors installed	Use as desired for “clean” AGND connection for discriminator/FADC chip; remove 0 ohm resistor to DGND plane, replace 0 ohm resistor to AGND plane with SMT inductor.
108	SVX QGND	Tied via 0 ohm resistors to AGND return plane and/or DGND return plane; nominally, both resistors installed	Use as desired for “clean” AGND connection for discriminator/FADC chip; remove 0 ohm resistor to DGND plane, replace 0 ohm resistor to AGND plane with SMT inductor.
83,84,70,69	VREF1 – VREF4	Four 0-3.5V DAC outputs controlled by AFE microprocessor. DACs are eight-bit (256 step) devices.	Use with internal resistor dividers to control reference voltage ladders of FADC chips.
121	VCLMP	Nominal 4.06V reference (resistor divider) derived from AVDD voltage source. (uses 1mA)	Not connected. Can remove resistors. Possible use as current source setting for new discriminator
82	CH_0_PA	Tied to –12V via 68K resistor.	Not connected
90	Priority_out	SVX BN pin, goes to TN of next MCM. Pin from last MCM goes to input pin of VSVX PLD.	Same function as in old MCM. Goes to FPGA for readout control, internally connected between FPGA and discriminator chip for download of discriminator parameters.

98-105	SVX DATA BUS	Eight bit tri-state data bus. Terminated to DGND on board.	Same function as in old MCM, except only used in Readout mode.
97	SVX DVALID	Tri-state line. Terminated to DGND on board.	Same function as in old MCM, except only used in Readout mode.
109	Priority_in	SVX TN pin. Pin of first MCM goes to output pin of VSVX PLD, also has 1K pullup to +5V.	Same function as in old MCM. Goes to FPGA for readout control, internally connected between FPGA and discriminator chip for download of discriminator parameters.
91	SVX VCAL	Analog voltage line, bussed across all MCMs, driven by SVX Sequencer from a ***loooong*** way away over a poorly grounded cable.	Not connected. Likely too noisy to be of use. VCAL functionality for testing is handled below.
92,93,94	SVX CHG_MOD,MODE1, MODE0	SVX mode control lines, common to all MCMs	Same function as in old MCM.
96	CLK	Positive half of PECL differential SVX clock	AFE board to be modified so that this becomes a TTL level signal. Goes to FPGA.
95	CLKB	Negative half of PECL differential SVX clock	Not connected.
114-118	SIFT Clocks	Five LVTTL signals, unique per MCM, from CLOCKGEN CPLD.	Still used as clocks but with radical new functions: • Pin 114: 53 MHz clock • Pin 115: 61 MHz clock • Pin 116: undriven, reserved • Pin 117: 7.6 MHz clock (PWM) • Pin 118: 7.6 MHz clock (sync)
75,126	SIFT VHDR	Nominal 3.00 V reference (resistor divider) derived from AVDD voltage source. (each consumes 1mA)	Not connected.
72,123	SIFT VLTH inputs	Two 0-2.5V DAC outputs controlled by AFE microprocessor. DACs are eight-bit (256 step) devices.	Used as “VCAL” equivalent for the two FADCs inside the new MCM.
71,125	SIFT VHTH inputs	Mirror voltages of the two VLTH voltages, which range from 2.5 to 5V as VLTH voltages range from 2.5 to 0 volts, such that difference between a VLTH and the VHTH goes from 0 – 5V with the centerpoint of the voltages always at 2.5V.	Not connected.
73,122	SIFT VHTH inputs	Two more VHTH voltages driven by independent DACs, both running from 2.5 to 5.0 volts.	Available as required for control voltages for new discriminator.
74,81,124	SIFT digital controls	Three digital signals, pulled up to +5V via 1K ohm resistors, controlled by open-collector outputs of VSVX_MUX CPLD.	VSVX_MUX CPLD to be removed, so will simply be three lines pulled up to +5V via resistors. No use in new MCM.

50 – 57	SIFT digital outputs	Re-used as parallel input data for programming download of FPGA	Driven by pins of LVDS_MUX CPLD.
151-160	SIFT digital outputs	Re-used as 10-bit LVDS data from FPGA	Received and redriven by LVDS_MUX CPLD to LVDS drivers on AFE board.
32 – 35	SIFT digital outputs	Re-used as FPGA programming control pins (CCLK, PROGRAM*, etc.)	Driven by pins of LVDS_MUX CPLD.
28-31, 36-45, 47-49, 58-64, 132-149, 161-168	SIFT digital outputs	Unused, no coneection	Not connected. Wisdom would suggest that any of these which can be easily connected to FPGA pins should be, to allow for extra controls, clocks, status, etc.